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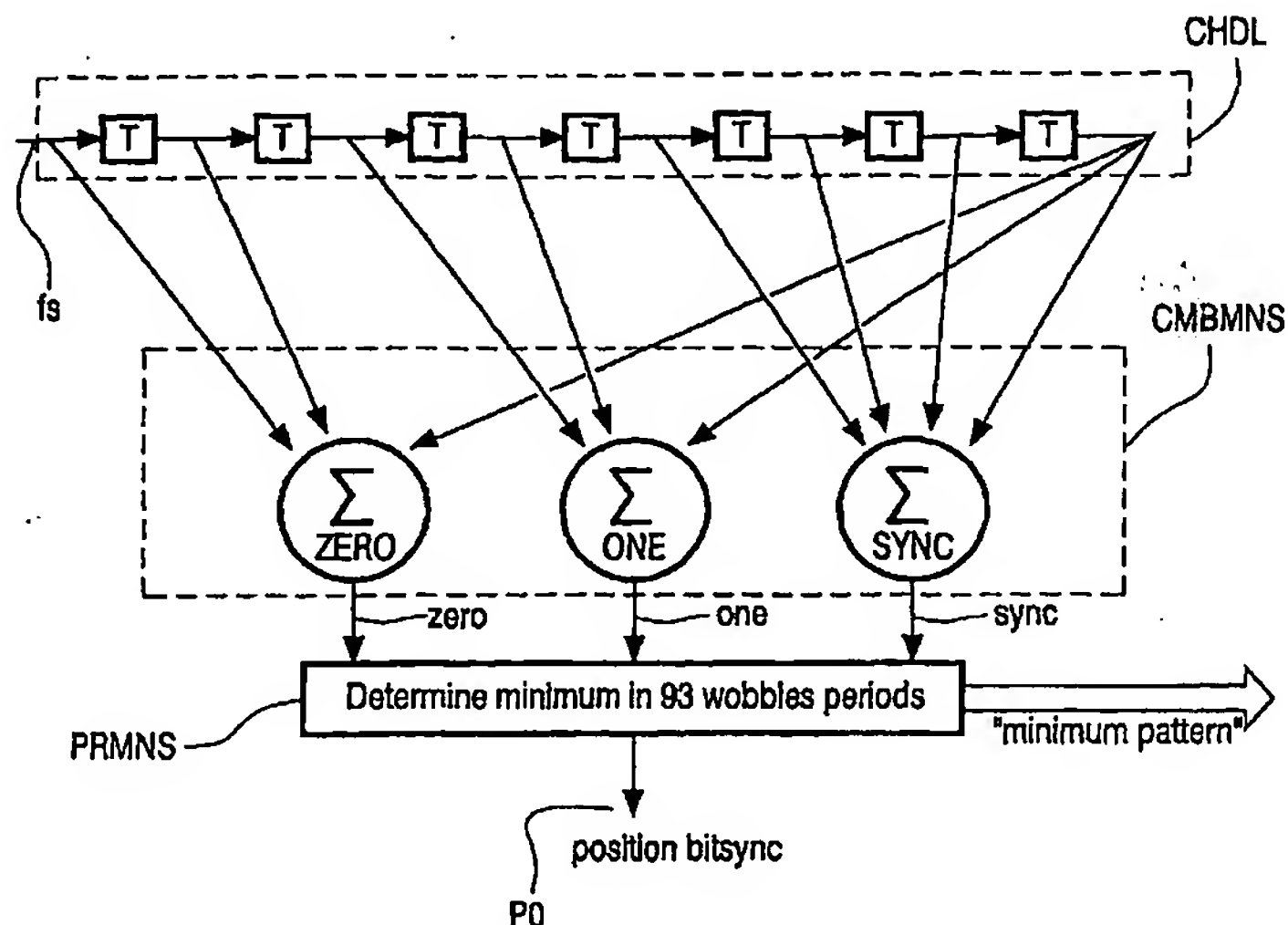
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(54) Title: BIT SYNCHRONIZATION DETECTION MEANS



(57) Abstract: Detection means for detecting information in a signal, comprising integration means for integrating the signal over time such that the integration means is periodically reset at about the start time reference of a periodic time interval; and a sample&hold circuit for periodically sampling and holding the integrated signal (int) at about an end time reference of the periodic time interval and thereby delivering a further signal (fs). The detection means further comprises a chain (CHDL) of signal time delay elements, an input of the chain (CHDL) being coupled to receive the further signal (fs); and combining means (CBMNS) having combining inputs coupled to signal taps of the chain (CHDL), such that the number of the combining inputs and the position of coupling the combining inputs to the signal taps of the chain (CHDL) correspond to the information in the signal.

WO 2004/107344 A1